REMARKS

Applicants respectfully request reconsideration of the application in view of the amendments set forth above and the following remarks.

Allowed Claims

Applicants acknowledge the indication of allowable subject matter in each of claims 34 through 36.

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations.
> M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on United States Patent 6,172,611 to Hussain et al. in View of United States Patent 5,675,297 to Gose et al.

Claims 1, 6-9, 14, 16, 17, 22, 24-27, 37-40, and 49 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 6,172,611 to Hussain et al. (hereinafter "Hussain") in view of United States Patent 5,675,297 to Gose et al. (hereinafter "Gose"). Applicants respectfully traverse this rejection as set forth below.

The following arguments were set forth in Applicants' prior response dated August 20, 2003. However, in the outstanding Office Action mailed November 7, 2003, the Examiner did not respond to any of the new arguments proposed by the Applicants in their response of August 20. Accordingly, the argument set forth by the Applicants in the August 20 response is repeated below in its entirety. As stated in the M.P.E.P.: "Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it." M.P.E.P. § 707.07(f) (emphasis added).

Hussain discloses an apparatus for monitoring the thermal state of a system. Column 2, Lines 60-67; Column 3, Lines 50-53. With reference to FIG. 1 of Hussain, a system 100 includes an embedded controller 110, a CPU chipset 120, a CPU 130 having a temperature sensor 132, a thermal management IC 140, a DC fan 160 and fan controller 150, and a power supply 170. Column 4, Lines 1-17. The temperature sensor 132 on CPU 130 is coupled with the thermal management IC 140, which includes its own on-board temperature sensor 146 for sensing a local temperature. Column 4, Lines 18-37. The embedded controller 110, which is controlled by the operating system of system 100, controls a CPU thermal management software module, with the assistance of chipset 120 and thermal management IC 140. Column 6, Lines 12-19.

The thermal management IC 140 includes a number of temperature setpoints, both software and hardware. Column 4, Lines 38-52. When a signal received from the CPU temperature sensor 132 (or from the on-board temperature sensor 146) indicates that a software temperature setpoint has been exceeded, the thermal management IC 140 issues an "ALERT#" signal to the embedded controller 110, and it is the embedded controller

110 that initiates any counter measures. Column 4, Lines 56-65; Column 7, Lines 21-66; FIG. 3. For example, the embedded controller 110 may direct the fan controller 150 to power up the fan 160, or the embedded controller 110 may direct the chipset 120 to throttle down the speed of a system clock signal 122 provided by the chipset to the CPU 130. Column 4, Line 65 through Column 5, Line 5; Column 5, Line 29 through Column 6, Line 8. When a signal received from the CPU temperature sensor 132 (or from the on-board temperature sensor 146) indicates that a hardware temperature setpoint has been exceeded, the thermal management IC 140 provides a shutdown signal to the power supply 170, and the power supply 170 then performs any necessary countermeasures (e.g., powering down the CPU 130). Column 5, Lines 13-22; Column 7, Lines 21-66; FIG. 3.

In sum, the CPU 130 includes a temperature sensor 132, but does not include any other elements of a thermal management system. Further, although the thermal management IC's on-board temperature sensor 146 may trigger countermeasures (see FIG. 3 of Hussain and accompanying text), those countermeasures are directed at the CPU 130. Thus, Hussain does not teach a thermal management system for an integrated circuit die, wherein the elements of the thermal management system are integrated on the die itself. Rather, Hussain teaches a thermal management system that is dispersed across multiple components of a computer system (e.g., the embedded controller 110, the chipset 120, the CPU 130, and the thermal management IC 140).

In contrast, the presently claimed invention is directed to a thermal management system for an integrated circuit die, wherein a temperature detection element, a power modulation element, a control element, and a visibility element of the thermal management system are all formed directly on the die whose thermal characteristics are being monitored. For example, claim 1 recites:

> 1. A thermal management system ***for an integrated circuit die*** comprising:
>
> a temperature detection element formed ***directly on the integrated circuit die***, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed ***directly on the integrated circuit die***, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor;

a control element formed ***directly on the integrated circuit die***, the control element including at least one register to provide an enable/disable bit for the thermal management system; and

a visibility element formed ***directly on the integrated circuit die***, the visibility element to indicate a status of the output of the at least one temperature sensor.

Each of claims 9 and 17 recites similar limitations. Also, claim 37 recites:

37. A method of forming a thermal management system ***for an integrated circuit die*** comprising:

forming a temperature detection element ***directly on the die***;

forming a power modulation element ***directly on the die***;

forming a control element ***directly on the die***; and

forming a visibility element ***directly on the die***.

The claimed invention has integrated a thermal management system (including a temperature detection element, a power modulation element, a control element, and a visibility element) onto the die whose thermal characteristics are being monitored, rather than distributing these elements across multiple discrete components as taught in the cited prior art, thereby eliminating some components (e.g., a separate thermal management IC 140, as disclosed in Hussain). It is respectfully noted that "**the omission of an element and retention of its function is an indicia of unobviousness**." M.P.E.P. § 2144.04(II)(B) (citing *In re Edge*, 149 U.S.P.Q. 556 (CCPA 1966)) (emphasis added).

The Examiner also cites the Gose patent. Gose discloses a conditional protection circuit 10 having a pulse-width modulation (PWM) circuit 12, a thermal shutdown circuit 20, and a TSD (thermal shutdown) detection circuit 16. Column 1, Lines 14-27; FIG. 1. However, Gose also fails to disclose, either individually or in combination with Hussain, the claimed thermal management system for an integrated circuit die.

In the telephone interview of July 18, the Examiner suggested that one of ordinary skill in the art would be motivated to modify the teachings of Hussain to arrive at the

claimed invention. More specifically, the Examiner suggested that it would be obvious to combine all of the components of Hussain's thermal management system (i.e., embedded controller 110, CPU chipset 120, CPU 130, thermal management IC 140, DC fan controller 150, and power supply 170) into an integrated thermal management system on a single IC chip. However, the Examiner's assertion is, respectfully, inconsistent with the disclosure of Hussain. As specifically stated in the SUMMARY section of Hussain:

> It has been discovered that a thermal management technique using a software and hardware programmable integrated circuit configured to receive a **remote temperature sensing** signal provides **the advantages of remote temperature sensing**, the flexibility of software programmability, and the reliability of hardware programmability. Column 2, Lines 41-46.

Clearly, as indicated in the passage above, Hussain is directed at and discloses only a temperature detection scheme wherein the temperature is sensed by a temperature sensor located remote from other components of the thermal management system. This reference does not disclose an integrated thermal management system having temperature detection, power modulation, control, and visibility elements all formed directly on the same die.

As noted above, Hussain discloses the use of a separate thermal management IC 140 for use in monitoring the thermal characteristics of a remote CPU 130 (see FIG. 1). It is stated in the specification of this patent that:

> One exemplary thermal management IC 140 is shown in FIG. 4. The TC1066 is available from [the assignee of the Hussain patent]. The TC1066 is a serially programmable, monolithic temperature sensor optimized **for monitoring modern high performance CPUs** with on-board integrated thermal diodes. Column 8, Lines 25-30.

This passage clearly indicates that the thermal management IC 140 is one component of a thermal management system for monitoring the thermal characteristics of a separate integrated circuit device – i.e., a "modern high performance CPU". It is also noteworthy that the aforementioned product (i.e., the "TC1066" thermal management IC)

is a product available from the assignee of the Hussain patent. The inventors and assignee of Hussain would certainly not intend, or suggest in their patent, that the disclosed thermal monitoring system be integrated onto the CPU itself, thereby eliminating the need for their own product.

In sum, Hussain contains no suggestion or motivation that its teachings be modified to arrive at the presently claimed invention. As the Court of Appeals for the Federal Circuit has warned:

> Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is **rigorous application** of the requirement for a showing of the teaching or motivation to combine [or modify] prior art references.
>
> ****
>
> Combining [or modifying] prior art references without evidence of such a suggestion, teaching, or motivation **simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability** – the essence of hindsight. *In re Dembiczak*, 50 U.S.P.Q.2d at 1617 (emphasis added).

As Hussain contains no suggestion or motivation that its disclosure be modified to arrive at the present claimed invention, it would seem the Examiner has engaged in hindsight reconstruction based upon the Applicants' disclosure.

In summary, the Hussain and Gose patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations. Therefore, a prima facie case of obviousness can not be made out with respect to claims 1, 9, 17, and 37 based upon the Hussain and/or Gose patents, respectively, and each of claims 1, 9, 17, and 37 is nonobvious in view of Hussain and Gose.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 6-8 are allowable as depending from nonobvious, independent claim 1. Similarly, claims 14 and 16 are allowable as depending from independent claim 9, claims 22 and 24 are allowable as depending from

independent claim 17, and claims 38-40 are allowable as depending from independent claim 37.

Obviousness Rejection Based on United States Patent 6,172,611 to Hussain et al. in View of United States Patent 5,675,297 to Gose et al. and Further in View of United States Patent 5,256,914 to Boomer

Claims 25, 26, 27, 31, and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hussain in view of Gose and further in view of United States Patent 5,256,914 to Boomer (hereinafter "Boomer"). Applicants respectfully traverse this rejection as set forth below.

Claim 25, as amended, recites:

> 25. A method comprising:
> providing an enable bit to a register to activate a thermal management system of a die;
> measuring a temperature on the die with a sensor of the thermal management system;
> providing a first state at an output of the sensor when the temperature is below a trip point;
> providing a second state at the sensor output when the temperature equals or exceeds the trip point;
> in response to the sensor output having the second state, engaging a power reduction mechanism for a specified time interval to reduce power consumption of the die;
> polling the sensor output after expiration of the specified time interval;
> **if the sensor output exhibits the second state when polled, repeating the acts of engaging the power reduction mechanism for the specified time interval and polling the sensor output after expiration of the specified time interval**; and
> if the sensor output exhibits the first state when polled, halting the power reduction mechanism.

Regarding the combination of Hussain, Gose, and Boomer, the Examiner states (Office Action, at page 4) that:

> The Hussain and Gose combination disclose a method including the subject matter discussed above except the use of time interval to reduce power consumption of the system, clock signal substantially equal to the last duty cycle of trip temperature, Boomer discloses the use of time interval to reduce power consumption of the system (col. 2, Lines 6-34, Col. 7, Lines 14-30), clock signal substantially equal to the last duty cycle of trip temperature (Col. 2, Lines 15-34) in order to prevent damage to the IC with fast response and fast return of the circuit to normal operation (Col. 2, Lines 30-34).

Firstly, it is unclear what specifically in Boomer discloses "the use of time interval to reduce power consumption," as Boomer discloses a method and circuit for protecting and output buffer circuit by detecting the occurrence of a short circuit condition. Column 2, Lines 36-41. Boomer does not disclose a thermal management system nor does this reference disclose a method of reducing power consumption of a die. Secondly, the embodiment claimed in claim 25 does not simply use a "time interval to reduce power consumption." Rather, claim 25 is directed to an embodiment in which a power reduction mechanism is engaged for one or more specified time intervals to reduce the temperature of a die.

More specifically, claim 25 recites a method wherein the output of a temperature sensor provides either a first state or a second state, depending upon the temperature of a die measured by the sensor. If the sensor output changes to the second state, which indicates the die temperature has exceeded a prescribed point (e.g., a trip point), a power reduction mechanism is engaged for a specified time interval. At the end of this time interval, the sensor output is polled, and if the sensor output state has not changed (e.g., to the first state, which would indicate the die temperature is below the trip point), the power reduction mechanism is again engaged for the same specified time interval. The acts of engaging the power reduction mechanism for the specified time interval and polling the sensor output upon expiration of this time interval are repeated so long as the sensor output remains at the second state (indicating the die temperature is above the trip point). If the sensor output is at the first state when polled upon expiration of one of the specified time intervals, the power reduction mechanism is halted. Claim 25 was

amended to clarify that the engagement of the power reduction mechanism for the specified time interval is repeated until the sensor output changes to the first state, which would indicate the die has cooled to a desired temperature (e.g., a temperature below the trip point).

Thus, as Hussain, Gose, and Boomer, either individually or in combination, fail to teach or suggest at least the above-noted limitations, a prima facie case of obviousness can not be made out with respect to claim 25 based upon these references. Accordingly, claim 25 is nonobvious in view of the combination of Hussain, Gose, and Boomer.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 26, 27, 31, 32, and 49 are allowable as depending from nonobvious, independent claim 25.

Claim Objections - Allowable Subject Matter

Claims 2-5, 10-13, 15, 18-21, 23, and 33 were objected to as being dependent upon a rejected base claim, but each of these claims would be allowable if rewritten in independent form. Office Action, at page 5. As set forth above, each of independent claims 1, 9, 17, and 25 is patentable in view of the cited prior art. Thus, Applicants submit that each of claims 2-5, 10-13, 15, 18-21, 23, and 33 is patentable as written in dependent form.

CONCLUSION

Applicants submit that claims 1-27, 31-40, and 49 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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